20.1 A 5GHz 108Mb/s 2×2 MIMO Transceiver with Fully Integrated +16dBm PAs in 90nm CMOS

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Multiple antenna transceivers offer the potential for high data rates and/or increased range in wireless systems [1]. In this paper, a fully integrated 2×2 MIMO transceiver is presented that supports both: (1) spatial diversity – where the same information is encoded into all transmit streams, thereby improving the range [2], and (2) spatial multiplexing – where each antenna transmits independent signals, thus improving the spectral efficiency. The emphasis of this paper is on doubling the data rate (54 to 108Mb/s) in the same 20MHz channel through spatial multiplexing. The 5GHz transceiver, implemented in a dual-oxide strained silicon 90nm CMOS process, incorporates: (1) two pairs of front-end (LNA and PA) matching networks on the top layer of a flip-chip package, (2) on-die +20dBm P_{1dB} linearized power amplifiers, (3) a frequency distribution scheme and floor-plan that minimize VCO pulling and MIMO crosstalk, and improve MIMO synchronization and (4) programmable bandwidth (10-100MHz) baseband filter/VGA sections that support a 4× increase in data rate through the use of fat channels (>20MHz bandwidth).

Figure 20.1.1 demonstrates the basic principle of spatial multiplexing. A high-rate bit stream is decomposed into multiple lower-rate bit streams which are transmitted from M (>1) antennas in the same frequency channel. The N (≥M) receiver antennas receive the superposition of signals originating from all transmitters. If the environment between TX and RX antennas is rich in multi-path, the N×M matrix $\underline{H}$ describing the channel is invertible and the RX can deconvolve the transmitted bit streams. In this way spatial multiplexing establishes multiple independent data pipes between TX and RX thereby increasing spectral efficiency [1].

In a single-chip MIMO implementation it is essential to minimize on-chip and package coupling between the radios. Coupling increases the correlation between the ideally independent data pipes, thereby reducing capacity and increasing BER. Figure 20.1.2 shows the architecture of the direct-conversion 2×2 MIMO transceiver based on [3]. The front-end (LNA and PA) passives are realized as microstrips on the top layer of a multi-layer flip-chip package to get a high Q and are placed at a maximum distance to reduce the coupling to less than -30dB.

The 5GHz LO is generated from an 8GHz synthesizer by division and single side-band mixing, to minimize pulling from the on-chip PAs. The LO is shared between the two transceivers to minimize the synthesizer power dissipation and chip area. A common LO also relaxes the overall phase noise requirements of the system by improving the pilot-assisted phase noise tracking at the receiver. Figure 20.1.2 shows the phasor representation of the pilot tones at the two receivers, where $\Delta\phi 1$ and $\Delta\phi 2$ are due to phase noise. If the LO is shared between the two transmitters, and the same holds for the receivers, then $\Delta\phi 1 = \Delta\phi 2$. An additional uncorrelated noise component (e.g., from thermal noise), corrupts the phase estimate. Averaging out the pilot estimates reduces the effect of these uncorrelated components, thus improving the accuracy of the phase noise tracking. In this design CMOS scaling is exploited and rail-to-rail CMOS buffer chains with low output impedance and high reverse isolation are used to minimize coupling through the common LO distribution.

The baseband circuitry consists of a 6^{th}-order g_m-C elliptic filter and a five-stage VGA with 54dB gain. The filter is programmable between 10 and 100MHz and the VGA gain is variable in 2dB steps.

Each transmitter consists of a quadrature up-conversion mixer and an on-chip PA. The mixer is a linearized transconductor driving a Gilbert quad. The two-stage, cascoded, pseudo-differential PA uses a combination of thin and thick gate (3.3V) devices to simultaneously achieve high gain and efficiency, and reliable operation. The output stage of the PA is biased in class-AB mode to achieve high power efficiency. OFDM signals with a large peak-to-average ratio modulate the input capacitance of the class-AB devices, thereby producing significant AM-PM distortion and degrading the transmit EVM. A varactor is used to introduce an opposite phase shift and eliminate AM-PM distortion (Fig. 20.1.3). A lookup table addressed by the IQ baseband data generates the correction signal to drive the varactor [4].

The 2×2 transceiver is tested using a custom MIMO modem implemented in software. The software generates MIMO OFDM signals and passes them through an appropriate model of a 2×2 radio channel. Random Rayleigh channels with 25ns rms delay spread, typical of office environments, are used during the testing. The resulting RF signals are then applied to the two receivers and the output is digitized, passed through timing and frequency synchronization routines, MMSE channel equalization [1], and Viterbi decoding. The MIMO demodulation is performed at low-IF (10MHz) due to the limited number of matched inputs available at the digitizer (2 instead of 4). Zero-IF demodulation for the legacy 1×1 mode degrades the NF by 1.5dB.

In legacy 54Mb/s mode, each receiver achieves a sensitivity of -75.5dBm (packet error rate (PER) of 10%) in the presence of additive white Gaussian noise (AWGN). Due to multi-path fading, this sensitivity degrades to -68dBm for a 25ns Rayleigh channel. In the 108Mb/s 2×2 MIMO spatial multiplexing mode the corresponding sensitivity is -62.5dBm (Fig. 20.1.4). In order to achieve the same data rate in the 1×1 mode using the same 20MHz bandwidth, the receiver would require a minimum average input power of about -50dBm. Thus, the 108Mb/s 2×2 MIMO transceiver has a 12.5dB SNR advantage over conventional 1×1 transceivers. The measured MIMO sensitivity is close to theoretical predictions which demonstrates the effectiveness of our isolation techniques.

Figure 20.1.5 shows the 5GHz transmitter constellation and spectral mask in 1×1 and MIMO modes. In legacy 1×1 mode the TX delivers an average power of +16dBm (EVM of -25dB) with an efficiency of 7%. In the 2×2 mode each PA delivers an average power of +13dBm while meeting the more stringent EVM of -27dB required for MIMO. The linearization allows the PA to operate at a small backoff from the P_{1dB} of 20dBm. The transceiver performance is summarized in Fig. 20.1.6. The 2×2 MIMO transceiver, fabricated in a 90nm CMOS process (Fig. 20.1.7), occupies a total die area of $18mm^2$.

Acknowledgements:
The authors thank Minnie Ho, N. Dinur, A. Biran, S. Sandhu, S. Somayazulu, H. Alavi, K. Holt, D. Steele, D. Martin, R. Wang, N. Yaghini, Jian Gong, C. Zhan, John Vu, D. Trammo, A. Crouch, and K. Kahn for their help.

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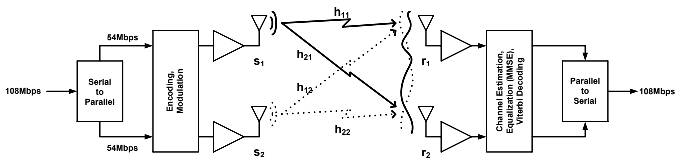

The signals at the receiver are given by

$$\begin{bmatrix} r_1 \\ r_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \cdot \begin{bmatrix} s_1 \\ s_2 \end{bmatrix}$$

which can be represented as

$$\underline{r} = \underline{\underline{H}} \cdot \underline{s} \quad \text{where} \quad \underline{\underline{H}} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix}$$

The receiver can estimate the two transmitted bit streams through the transformation :

$$\underline{\hat{s}} = (\underline{\underline{H}}^{*} \cdot \underline{\underline{H}})^{-1} \cdot \underline{\underline{H}}^{*} \cdot \underline{r}$$

Figure 20.1.1: Spatial Multiplexing increases spectral efficiency: the two transmitters send independent bit streams on spatial channels; the receivers estimate and equalize channel to deconvolve the bit streams.

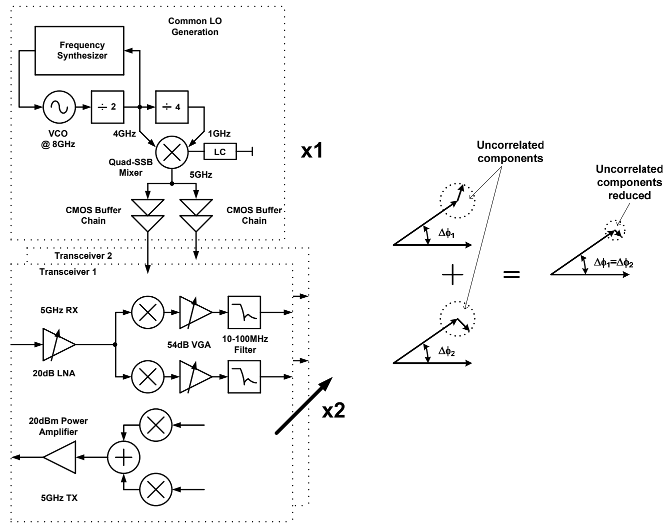

Figure 20.1.2: 5GHz 2x2 MIMO transceiver with common LO generation. Joint phase estimation improves the accuracy of phase tracking and synchronization.

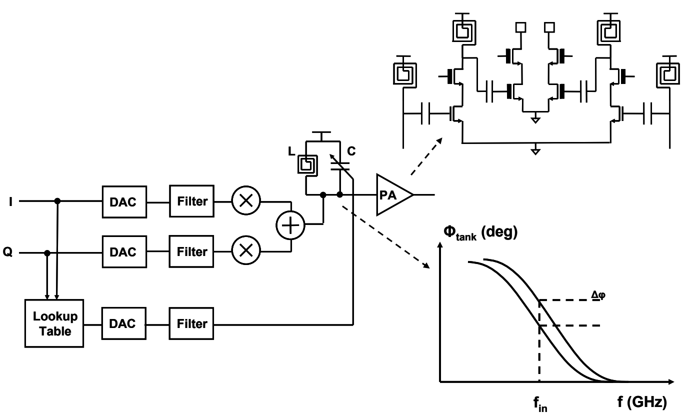

Figure 20.1.3 A varactor controlled by the baseband IQ data is used to counteract the signal-dependent phase shift that is responsible for AM-PM distortion in the PA.

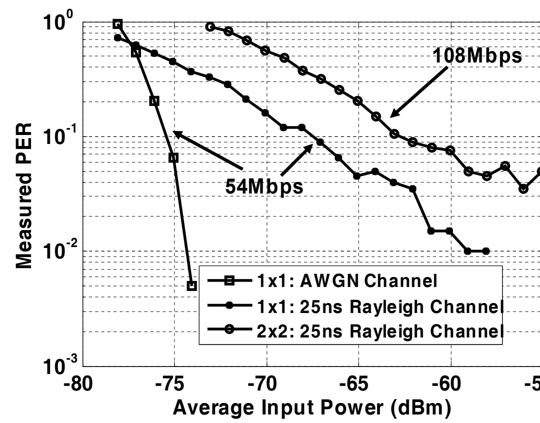

Figure 20.1.4: Measured PER as a function of average received power. Receiver measurements were performed at low-IF (100MHz).

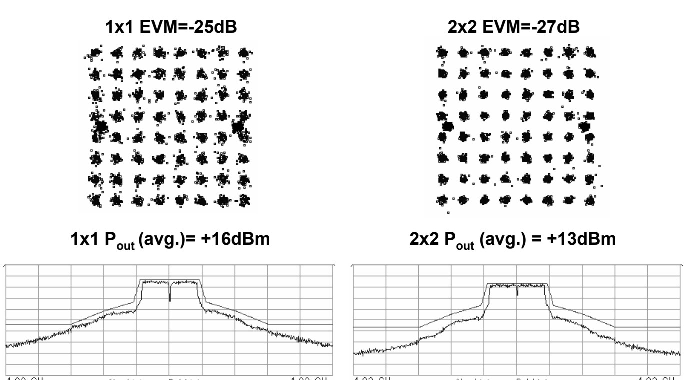

Figure 20.1.5 Measured TX constellation and spectral mask: +16dBm (avg.) for -25dB EVM in 54Mb/s 1x1 mode; +13dBm (avg.) each for -27dB EVM in 108Mb/s 2x2 MIMO mode.

5GHz RX Noise Figure	6dB
5GHz RX Sensitivity (54Mbps)	-75.5dBm (AWGN channel) -68dBm (25ns Rayleigh)
5GHz RX Sensitivity (108Mbps)	-62.5dBm (25ns Rayleigh)
RX IIP3	-12dBm
RX Power Dissipation	1x1 Mode: 170mW (1.4V) 2x2 Mode: 280mW (1.4V)
5GHz TX Average Power (64-QAM)	1x1 Mode: +16dBm (EVM: -25dB) 2x2 Mode: +13dBm (EVM: -27dB)
5GHz TX Power Dissipation	1x1 Mode: 840mW (1.4/3.3V) 2x2 Mode: 1400mW (1.4/3.3V)

Figure 20.1.6: Transceiver performance summary. Receiver measurements are performed at low-IF (10MHz); Zero-IF will degrade receiver performance by 1.5dB.

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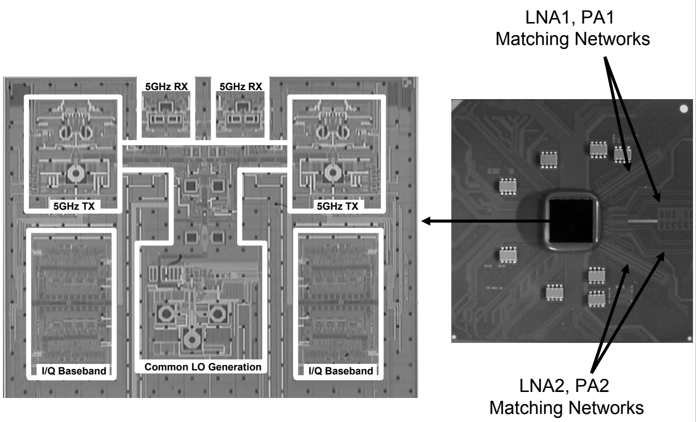

Figure 20.1.7 Die micrograph of 5GHz 2x2 MIMO transceiver in 90nm CMOS with front-end matching networks on top layer of flip-chip package.

